ABSTRACT OF THE DISCLOSURE

When a code word sequence is generated by converting input data words of **p** bits into code words of **q** bits and concatenating adjacent ones of the code words with a merge bit sequence of **r** bits in order to obtain the best DSV value, according to one aspect, the adjacent code words are concatenated with the merge bit sequence of **r** bits which is selected, free from the restriction of the minimum run-length of (d+1)T and the maximum run-length of (k+1)T based on the run-length limiting rule RLL(d, k) but permitting the minimum run-length of (d+1)T and the maximum run-length of (k+2)T. According to another aspect, a merge bit sequence to be inserted after a current code word is selected by prefetching the current code word, a next code word, and a further next code word, temporarily concatenating these code words with merge bit sequences of **r** bits respectively to prepare code word sequence candidates free from the predetermined run-length limiting rule, calculating the DSV values of the code word sequence candidates, selecting one of the code word sequence candidates having a DSV value whose absolute value is closest to zero, and selecting the merge bit sequence between the current code word and the next code word of the selected merge bit sequence candidate. According to a further aspect, the input data words are encoded by a p-q modulation scheme after introducing for a predetermined period, as an input data word, specific data comprising alternating current signals or direct current signals which would cause a modulation device that prefetches only the next code word to output a code word sequence which includes particular frequency components.